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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,316	07/11/2003	Patrick Lysaght	X-1410 US	4779

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XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/618,316	LYSAGHT ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 1958*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/21/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/618,316 and RCE with submission of IDS filed on 12/21/2005. Claims 1-41 remain pending in the application.

2. IDS: Note that applicant is requested to provide specific date of each of the references cited in the cited PTO/SAB/08A (10-01).

3. Examiner has treated the claims filed on 8/19/05.

Claim Objections

4. Claim 38 is objected to because of the following informalities: "An integrated circuit" is suggested to --A programmable logic device--; and "a crossbar switch" to be --a multi-stage crossbar switch having at least three-stages--. The suggested changes provide that all claims refer to the same invention of at least three-stages of a multi-stage crossbar switch implemented in a PLD. Appropriate correction is required. Examiner has examined the claim based on this suggestion.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-41 rejected under 35 U.S.C. 103(a) as being obvious over Ian Kyles, "Creating Large Switch Fabrics using the Three-Stage (Clos) Architecture", Copyright VITESSE Semiconductor Corporation, pp. 1-12 in view of Young et al., "A High I/O

Reconfigurable Crossbar Switch," pp. 1-8 or Insenser Farre et al. (Insenser) (applicable claims as shown in the rejection) (6,460,172).

7. As to claim 1, Kyles teaches at least three stages crossbars switch having first interconnections and second interconnection, first stage has inputs/output, second stage has inputs/outputs and third stage has inputs/outputs, where the inputs and outputs are one-to-one connection and can be changed providing inputs and outputs connections (Fig. 2, 3, 4, 5, 6, 7, 8 and 9-10). Kyles does not teach reconfiguration part. It is well known in the art that crossbar switches have been implemented on FPGAs (programmable logic device or PLD). Thus, Kyles teaches all claim limitation except reconfiguration part. Young et al. teach that (page 1), where crossbar switch (FPGA) is dynamically reconfigured or partially configured to select the input without effecting operation of other parts within the FPGA using embedded processor as suggested (see paragraph 3, 6 and 9). In addition, Insenser teaches an embedded microprocessor (processor) is used to configure and dynamically reconfigure partially or all the programmable features (CLBs, LUTs within FPGA or device) without the operation of the device at all (col.1 line 52 to col. 2 line 21; col. 5 lines 3-33; col. 5 lines 54-67; col. 6 lines 1-25). A great number of applications based on dynamic reconfiguration could also be identified and implemented with FIPSOC digital hardware including communication switches (col. 6 lines 7-25). With motivation as described above, practitioners in the art at the time the invention was made to modify the multi-stage crossbar switches as taught by Kyles and implement them on FPGAs using embedded processor as taught by Young or Insenser because the modified multi-stage crossbar

switches implemented on FPGA having embedded processor thereon configure and dynamically reconfigure partially or all the multi-stage crossbar switches providing selection of inputs and outputs without stopping or effecting the operation of the programmable logic device at all. This modified provides an expect result at least as taught by Insenser (col. 2 lines 1-21).

8. As to claims 22 and 34, remarks set forth in rejecting claim 1 equally apply.

9. As to claims 28, 31, 36 and 38, remarks set forth in rejection of claim 1 apply because of the a combination of teachings as described above would produce a multi-stage crossbar switch implemented on programmable logic device as recited in the claims.

10. As to claims 2-6, at least Figs. 7-8 (Kyles) show the claim limitations. Figs. 7-8 show at least three stages of a multi-stage crossbar switch, each having inputs/outputs and interleaved with interconnections (first interconnects and second interconnections formed interconnection region; second crossbars disposed there between; first and third crossbars are not disposed within the interconnection region; crossbars are arrayed as shown).

11. As to claims 7 and 10, Young teaches implementing switches (multi-stage crossbar switch) on FPGA (programmable logic device), where the programmable logic device includes configuration logic blocks (CLBs), where a first set of the first portion of the CLBs configured to provide input flip-flops (I-Mux) and a second set of the first portion of the CLBs configured to provide multiplexers and output flip-flops (O-Mux) (paragraphs 3 & 6). Insenser also teaches the applications of his system for

dynamically reconfigured the digital device (programmable logic device or FPGA) include communication switches (col. 6 lines 19-25; Fig. 1).

12. As to claims 8 and 29, Young teaches configuration controller circuit specifying an input-to-output connection and determines the I-Mux/O-Mux resources that need to be modified (at least paragraphs 3 & 6).

13. As to claim 9, Young teaches using double-length lines connection and configuration controller circuit to specify an input-to-output connection (inserting or connecting, removing or decoupling) (at least paragraphs 3 & 6).

14. As to claims 11-15, Young teaches the crossbar switches implemented on FPGA includes I-Mux/O-Mux, and pipelining data between stages for intra-crossbar processing as described in paragraph 3 (see layout and pipelining section 3.3).

15. As to claims 16-18 recite a first set of second portion of the CLBs and a second set of the second portion of the CLBs for the second stage of the crossbar switch; claims 19-21 recite a first set of third of the CLBs and a second set of the third portion of the CLBs for the third crossbar switch. Remarks set forth in rejecting claims 7-9 equally apply because a three stages of crossbar witch is implemented on FPGA, where each of the crossbar switch for each has the same configuration for providing the same latency as suggested by Young (teaching of latency equalization).

16. As to claims 23-26, Young teaches I-Mux and O-Mux configured to provide inputs to outputs connections using configuration controller circuit (see paragraphs 3 & 6). In addition, Insenser teaches configure and dynamically reconfigure the

programmable features within FPGA applicable in communication switches without effecting the operation of the device as described in above rejection of claim 1.

17. As to claim 27, Young teaches partial reconfiguration controller (Fig. 7 and paragraph 6). In addition, Insenser teaches a system including embedded processor, memories and programmable features within FPGA to configure and dynamically reconfigure partially or wholly the programmable features within the FPGA using configuration information stored in memories without effecting the operation of the device (Figs. 1, 4).

18. As to claim 30, Young teaches latency equalization to maintain constant clock latency across all paths using partially configurable delay registers in Figs. 5 and 6 (section 3.2).

19. As to claims 32-33 and 35, Young teaches partial reconfiguration controller operable by a user to specify inputs/outputs connections (paragraphs 3 & 6).

20. As to claim 37, Young teaches partial reconfiguration controller operable by a user to specify inputs/outputs connections (paragraphs 3 & 6).

21. As to claim 39 at least Figs. 7-8 of Kyles show configurable interconnects coupling inputs to outputs of the multi-stage crossbar switch. Young also implementing crossbar switches on FPGA using I-Mux and O-Mux and partial reconfiguration controller to specify connections between stages of the multi-stage crossbar as described (paragraphs 3 & 6).

22. As to claims 40-41, Young suggests using embedded processor to reconfigure the FPGA through the Internal Configuration Access Port (ICAP). Insenser also

teaches using embedded processor to configure and dynamically reconfigure the programmable features within FPGA without effecting the operation of the device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

VUTHE SIEK
PRIMARY EXAMINER